33.4 A Dual-Channel Direct-Conversion CMOS Receiver for Mobile Multimedia Broadcasting

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The growing market in streaming video to mobile phones has generated interest in technologies that will enable cost-effective delivery of multimedia to cell phones [1]. A recent advance in those technologies is the development of a MediaFLO system, which has been designed to efficiently distribute mass volumes of high-quality multimedia content to mobile subscribers. In this paper, the receiver circuit that is used in this system is described. It operates from 698MHz to 746MHz, a spectrum allocated by the FCC for advanced mobile services. In the USA, this corresponds to TV channels 52 to 59 in the UHF band. The receiver supports an OFDM physical layer with modulation ranging from BPSK for pilot carriers to 16-QAM for high-rate data carriers. This OFDM physical layer is capable of delivering a data rate up to 11.2Mb/s in a mobile environment.

Figure 33.4.1 shows the system block diagram of the dual-channel receiver. Because of the severe transmit power levels from analog broadcast systems, channel-selective SAW filters are needed to suppress the adjacent channel jammers before the LNA. Futhermore, to enhance the amount of content available, the receiver supports two channels, which explains the need for two input channels. Each LNA needs to cover the entire band of interest, since the specific channels assigned by FCC can vary by geography. SAW filters, being off-chip, are changed by phone manufacturers. The receiver needs to operate with a maximum input power level of -17dBm as defined at the RFIC input and has a sensitivity level of -100dBm.

The receiver utilizes a direct-conversion architecture (Fig. 33.4.2), consisting of two LNAs, an on-chip transformer, downconversion mixers, baseband I/Q filters, and a frequency synthesizer. In addition, there is a state machine that controls the slotted wake up. The receiver is required to operate simultaneously with a regular mobile call with no degradation in performance. Therefore, severe jamming conditions need to be considered, including transmit signals for mobile calls and adjacent channel interference such as existing analog broadcast systems. The jammer signals are attenuated by the channel-specific SAW filter and by the analog and digital baseband filter. The incoming RF signals from the antenna pass through their respective SAW filters and LNAs. The dedicated LNAs avoid lossy off-chip RF switches. The two receive signal paths are combined at the input of the RF mixers by sharing the same transformer. Only one receive signal path is active at any one time. The baseband signal is filtered by a low-pass filter. The receive-chain dc-offset is cancelled using two low-speed 8b DACs and the IIP2 performance is significantly improved using an IM2 calibration circuit.

The cascode LNA makes use of the modified derivative superposition (MDS) technique [2] as depicted in Fig. 33.4.2. Two input FETs are in parallel, one biased in strong inversion and the other in sub-threshold. By properly choosing the device size, degeneration inductors, and bias current, their IM3 components can be cancelled, leading to higher IIP3. An on-chip transformer with a high coupling coefficient is used to convert the single-ended signal to a differential signal in current mode. The transformer also achieves additional current gain by adding resonant capacitors. The primary inductance is 13.3nH and the secondary is 2.9nH. The primary Q is 6.2 and the secondary 5.4. The turn ratio is 2.1 and the coupling coefficient is 0.8. A double-balance Gilbert-cell mixer is adopted for downconversion. It has a common-gate input and capacitive cross-coupling to boost transconductance. Since the LNA-mixer interface is on-chip, the input impedance is no longer limited to 50Ω, and is optimized to achieve maximum current gain.

The receiver baseband filters implement a 7^{th}-order Chebyshev low-pass characteristic with a cutoff frequency of 2.8MHz. The filter contains a single real-pole stage followed by three cascaded biquad stages. The filter implements a transimpedance transfer function taking the current-mode signals from the mixer output nodes and converting them to voltages at the filter output pins. Each stage of the filter is implemented as active-RC architecture. The measured frequency response of the filter over process and temperature variations for the interested bandwidth shows a passband ripple of less than 0.5dB.

A conventional type-II integer PLL with a phase switching prescalar is integrated to synthesize the LO. The required LO frequencies range from 701MHz to 743MHz in a 6MHz grid and the VCO oscillates at four times the LO frequency. A frequency divider is used to produce I and Q components of the LO. The VCO is an LC tuned oscillator with the stacked NFET-PFET differential pair for negative resistance. This architecture achieves low phase noise with high power efficiency [3]. The LC resonator uses spiral-inductor and MOS varactors. The tuning range of the VCO is augmented by linear thermometer-coded coarse-tune capacitor bank, which is made of metal-oxide-metal (MOM) capacitors arranged as vertical parallel plates (VPP) to achieve a more compact layout (Fig. 33.4.3). This array of discrete capacitors is tuned by a digital state machine that calibrates the VCO before the fine tuning. The VCO achieves 33% tuning range which is more than wide enough to track phase-lock across process and temperature variations. The closed-loop phase-noise performance measured at the LO frequency is shown in Fig. 33.4.4.

There are two timing modes for this OFDM receiver: acquisition mode and slotted mode. The receiver enters acquisition mode upon power-up. The slotted mode is when the receiver is powered and switches between “active” and “sleep”. An internal timer, which consists of a finite state machine and programmable counters, is designed to accurately control the timing of various calibrations and the turn-on of the individual blocks.

The IC is implemented in a 0.25μm RFCMOS process. It occupies a total silicon area of $7mm^2$ and is packaged in a 32-pin QFN package. The received OFDM signal response in the baseband is shown in Fig. 33.4.5. The measured performance is summarized in Fig. 33.4.6 and the chip micrograph is shown in Fig. 33.4.7. The system performance is validated using a MediaFLO demodulator, both on stretched and form-factor accurate experimental phone platforms.

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References:
[1] P. Antoine, *et al.* “A Direct-Conversion Receiver for DVB-H,” *ISSCC Dig. Tech. Papers*, pp. 426-427, Feb., 2005.
[2] V. Aparin, *et al.* “A Fully Integrated Highly Linear Zero-IF CMOS Cellular CDMA Receiver,” *ISSCC Dig. Tech. Papers,* pp. 324-325, Feb., 2005.
[3] Y. Wu, V. Aparin, “A Monolithic Low Phase Noise 1.7GHz CMOS VCO for Zero-IF Cellular CDMA Receivers,” *ISSCC Dig. Tech. Papers*, pp.396-397, Feb., 2004.

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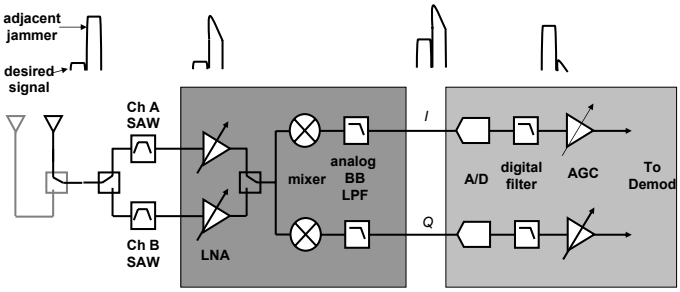

Figure 33.4.1: System block diagram.

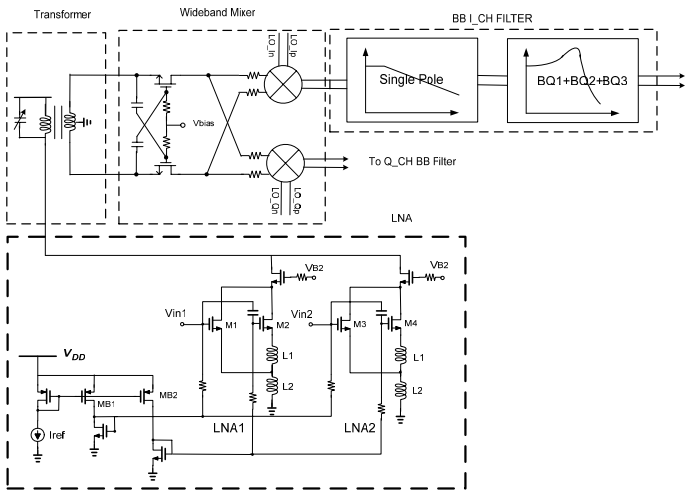

Figure 33.4.2: Simplified schematic of the signal path.

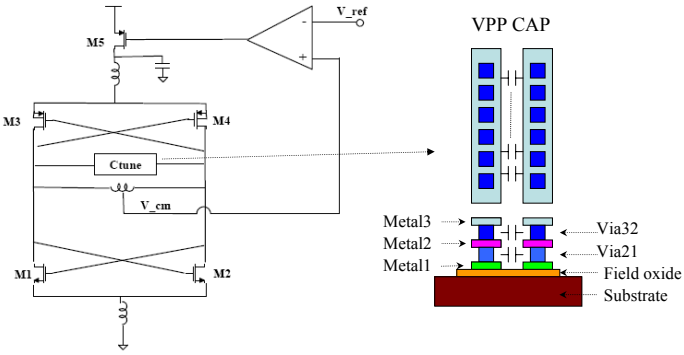

Figure 33.4.3: VCO schematic and VPP-cap top view and cross section.

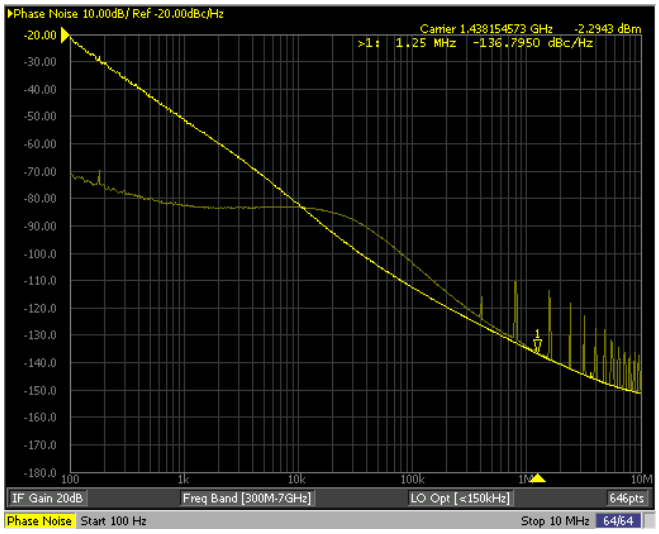

Figure 33.4.4: VCO/PLL phase-noise performance at VCO/2.

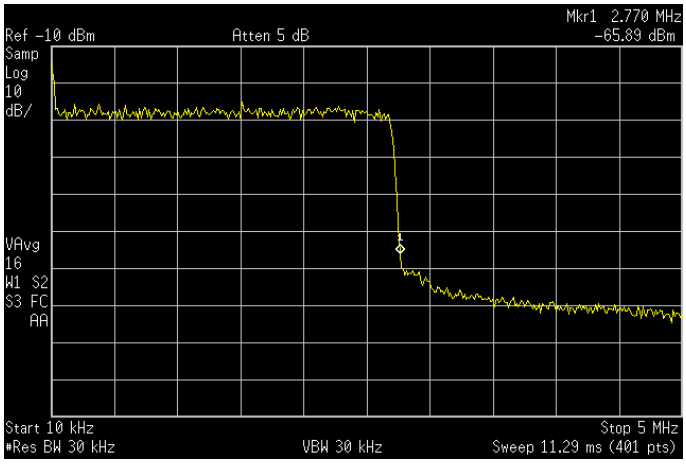

Figure 33.4.5: Receiver response.

Signal path	
Input frequency	698MHz – 746MHz
Voltage Gain (max gain state)	54dB
Noise Figure	2.6dB
IIP3 (out-of-band jammer)	-5.5dBm
Synthesizer	
Phase noise at 100KHz offset	-110dBc/Hz
Phase noise at 1MHz offset	-140dBc/Hz
Integrated phase noise (1KHz – 2.71MHz)	-37.5 dB
Lock time	330µs
Reference Spur	-66dBc
Full receiver	
Sensitivity	≤ -100dBm
Power	61mA @ 2.6V

Figure 33.4.6: Measured performance summary.

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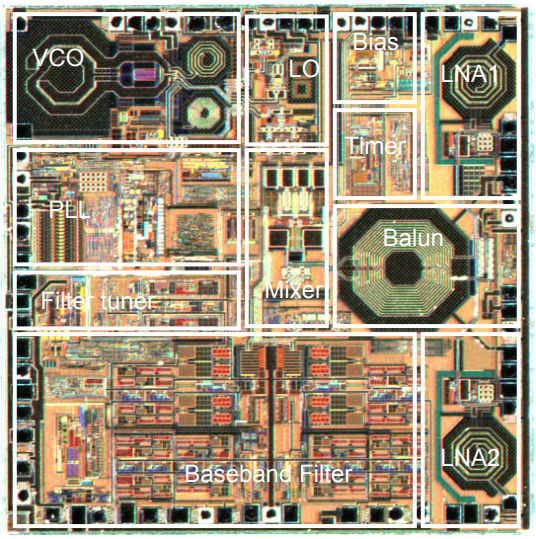

Figure 33.4.7: Chip micrograph.

